

Fig. 1

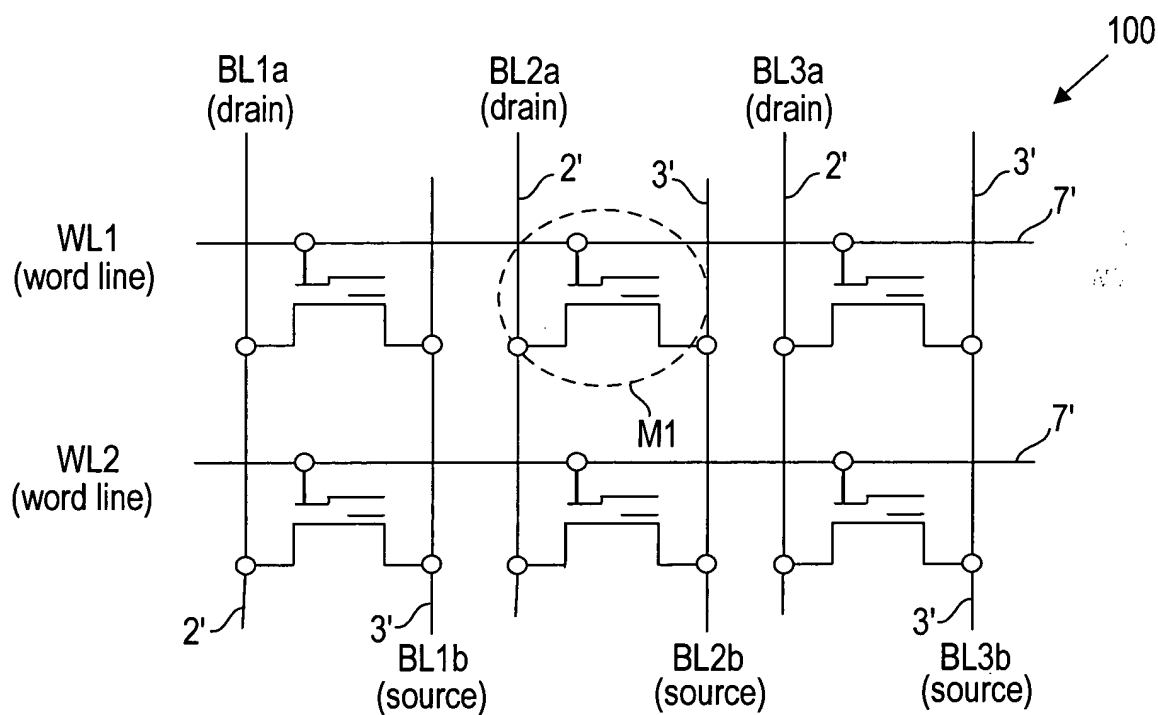


Fig. 2

Table 1

|       | BL1a | BL1b | BL2a | BL2b | BL3a | BL3b | WL1  | WL2   |
|-------|------|------|------|------|------|------|------|-------|
| Erase | F    | F    | F    | F    | F    | F    | -Vpp | 0     |
| Write | Vppx | F    | 0    | F    | Vppx | F    | Vpp  | <Vppx |
| Read  | Vr   | 0    | Vr   | 0    | Vr   | 0    | ~Vcc | 0     |

Note:  $V_{ppx} < V_{pp}/2$ ,  $V_r \sim 1V$

Fig. 2a

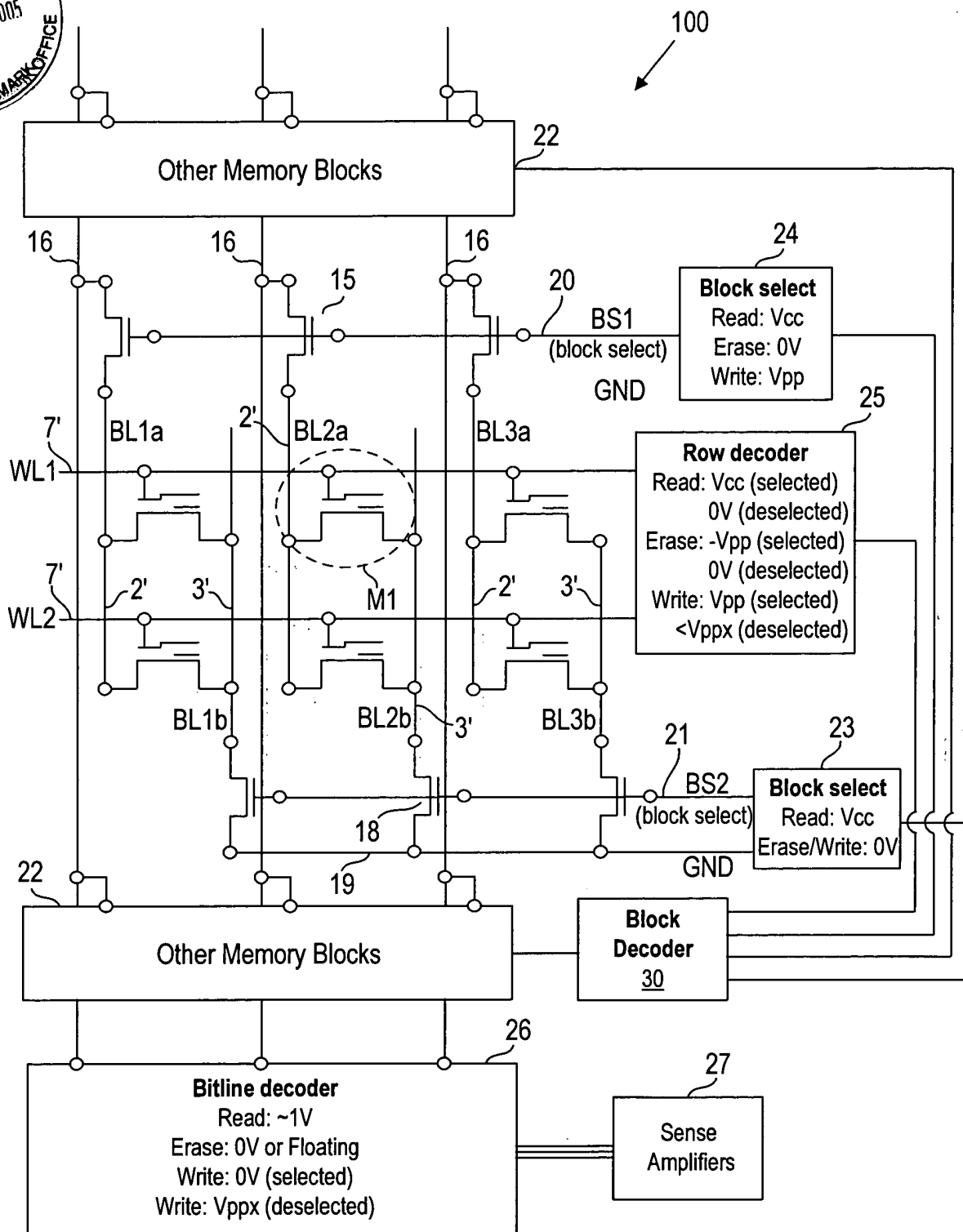


Fig. 3



Fig. 4a

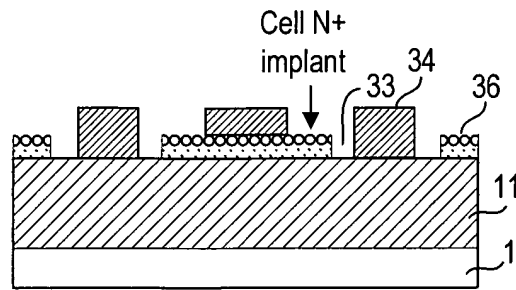


Fig. 4b

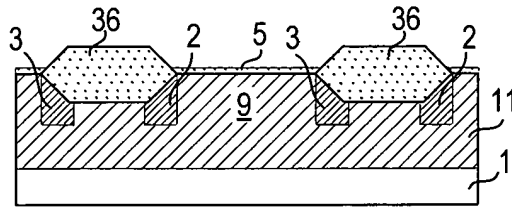


Fig. 4c

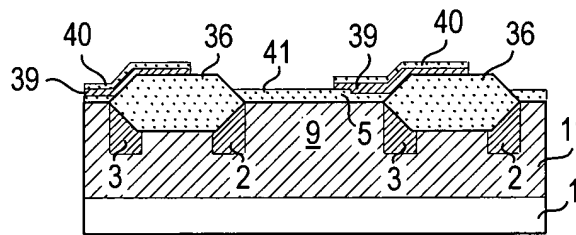


Fig. 4d

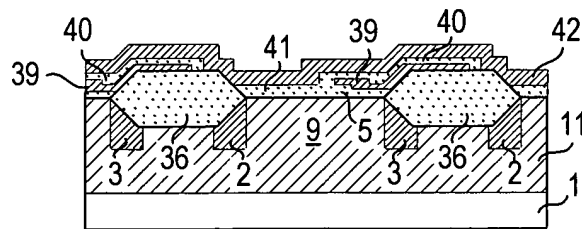
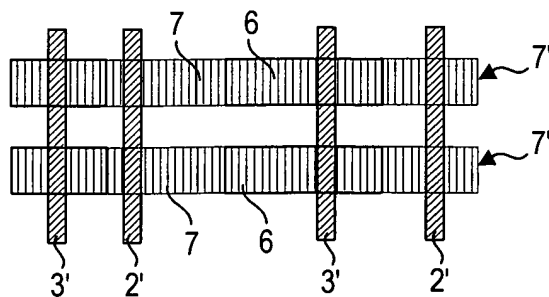


Fig. 4e



A cross-sectional view of a semiconductor device. A substrate 1 is covered by a thin layer 2. A gate stack 3 is formed on the surface. A gate 4 is formed on top of the gate stack 3. A channel 9 is formed in the substrate 1 under the gate 4. Source and drain regions 36 are formed in the substrate 1 on either side of the channel 9. A first S/D angle implantation 45 is performed into the source and drain regions 36 at an angle. A second S/D angle implantation 46 is performed into the source and drain regions 36 at a different angle. A third S/D angle implantation 45 is performed into the source and drain regions 36 at a different angle. A fourth S/D angle implantation 46 is performed into the source and drain regions 36 at a different angle. A fifth S/D angle implantation 45 is performed into the source and drain regions 36 at a different angle. A sixth S/D angle implantation 46 is performed into the source and drain regions 36 at a different angle.

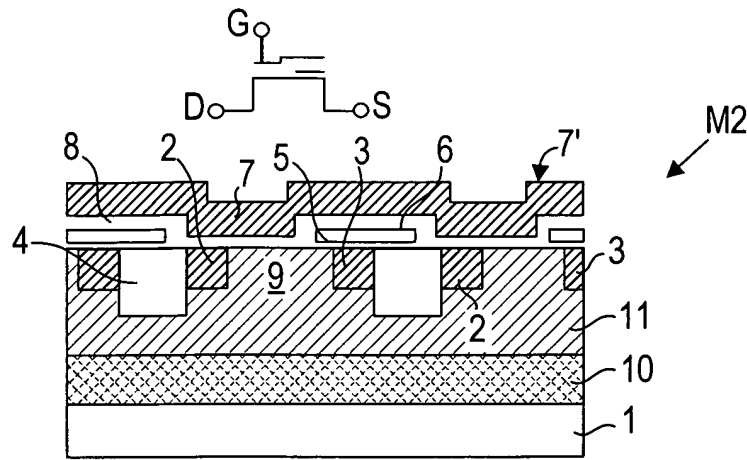


Fig. 6

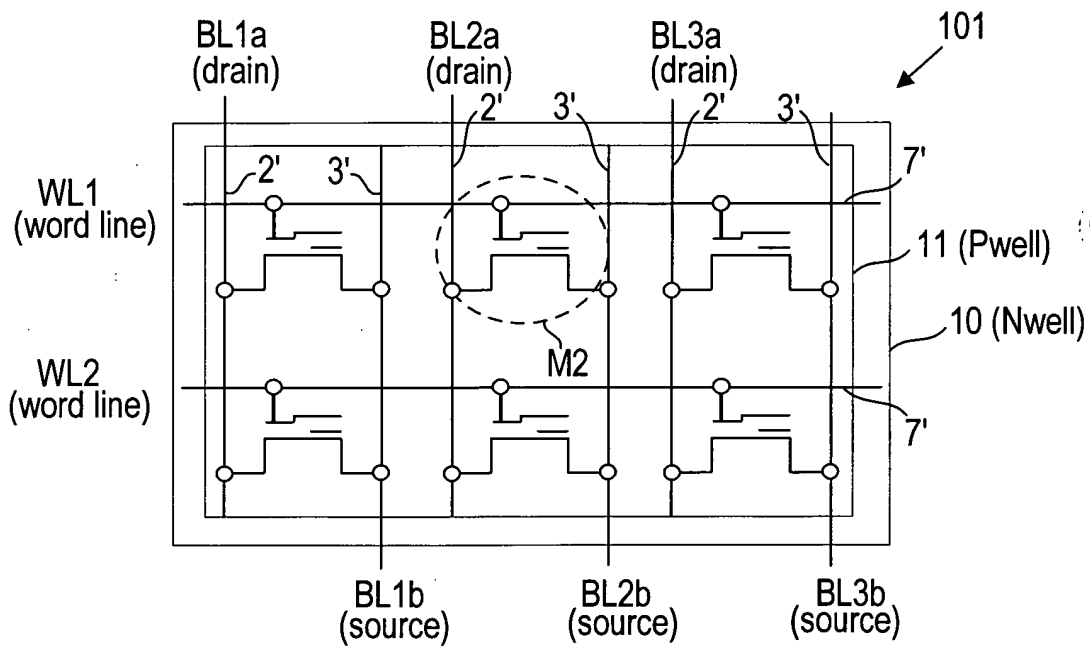


Fig. 7

Table 2

|       | BL1a             | BL1b | BL2a           | BL2b | BL3a             | BL3b | WL1              | WL2               | Pwell           | Nwell           |
|-------|------------------|------|----------------|------|------------------|------|------------------|-------------------|-----------------|-----------------|
| Erase | F                | F    | F              | F    | F                | F    | 0                | V <sub>pp</sub>   | V <sub>pp</sub> | V <sub>pp</sub> |
| Write | V <sub>ppx</sub> | F    | 0              | F    | V <sub>ppx</sub> | F    | V <sub>pp</sub>  | <V <sub>ppx</sub> | 0               | 0               |
| Read  | V <sub>r</sub>   | 0    | V <sub>r</sub> | 0    | V <sub>r</sub>   | 0    | ~V <sub>cc</sub> | 0                 | 0               | 0               |

Note: V<sub>ppx</sub> ≤ V<sub>pp</sub>:2, V<sub>r</sub>~1V

Fig. 7a

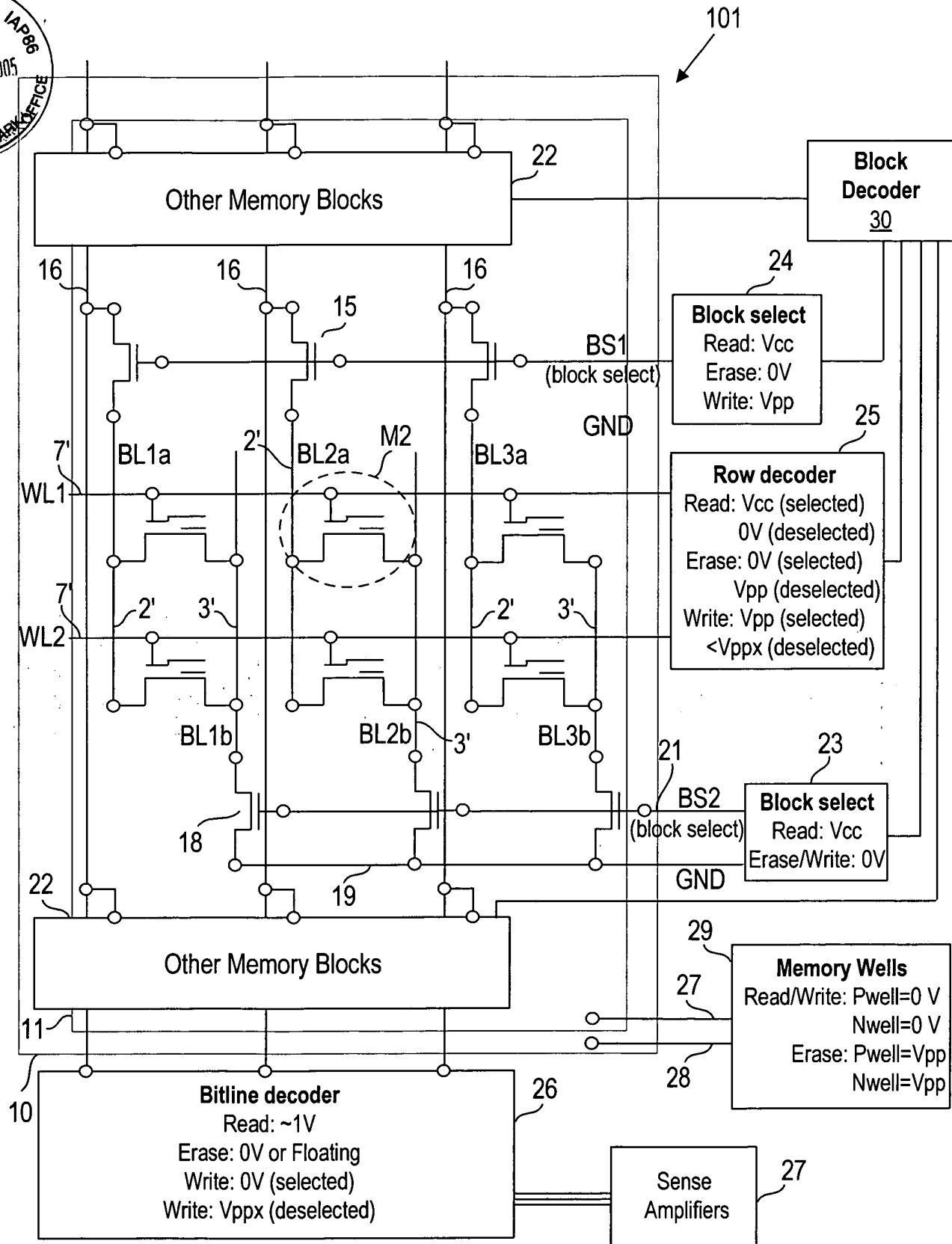
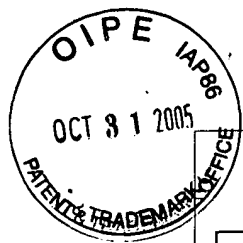


Fig. 8



Fig. 9a

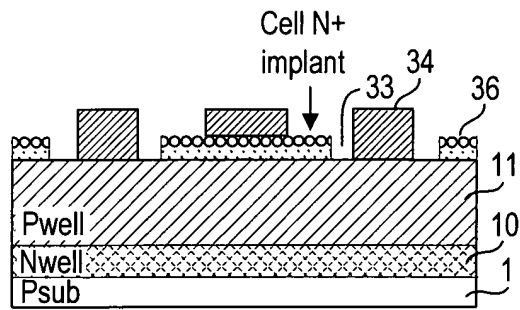


Fig. 9b

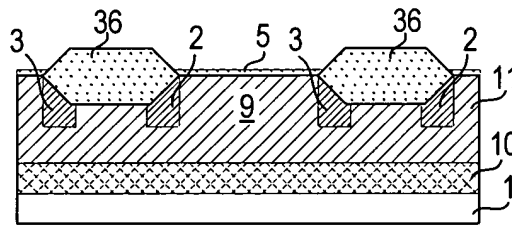


Fig. 9c

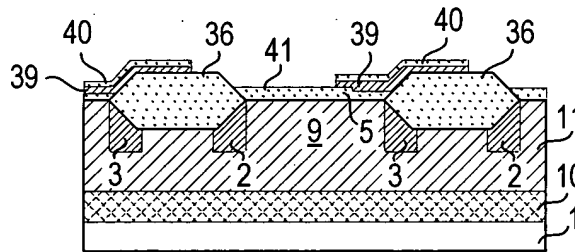


Fig. 9d

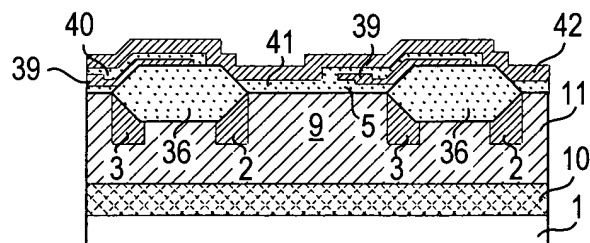


Fig. 9e

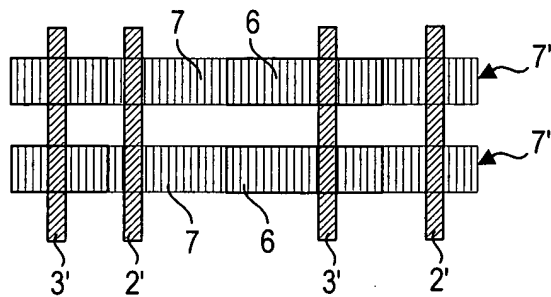




Fig. 10a

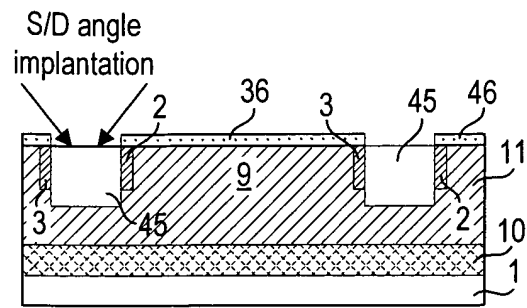


Fig. 10b

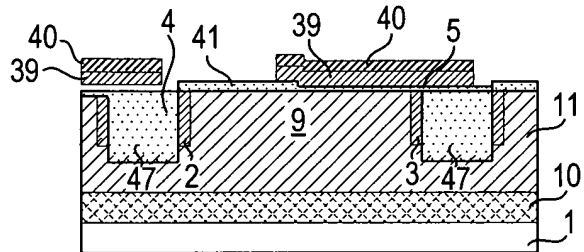


Fig. 10c

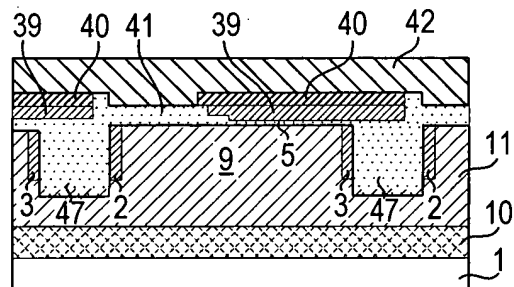


Fig. 10d

